Remarks

I. Status of Claims

Claims 1-25 were pending.

Claim 1 has been amended.

Previously withdrawn claims 14-21 have been canceled without prejudice.

The Examiner has indicated that claims 23 and 25 would be allowable if rewritten in independent form.

II. Claim Rejections

A. Independent Claim 1

Independent claim 1 has been amended and now recites that alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures *respectively* supported by *different* integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range.

The Examiner has rejected independent claim 1 under 35 U.S.C. § 103(a) over Ho (U.S. 4,254,445) in view of Yao (U.S. 6,163,068), Ferri (U.S. 4,326,180) and Houston (U.S. 6,362,117). The cited references, however, taken alone or in any permissible combination, do not teach or suggest all of the features of the inventive common carrier now recited in independent claim 1. It is noted that the Examiner's discussion regarding the construction of product by process claims does not apply to independent claim 1 because the claim is not defined with respect to any process.

1. Ho

Ho fails to teach or suggest a common carrier in which alignment between the integrated chip substrates bonded to a carrier substrate is within a first alignment tolerance range and alignment between the integrated structures *respectively* supported by *different* integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as now recited in independent claim 1. Indeed, in Ho's approach, integrated structures are formed on substrates to form individual LSI chips, and the individual LSI chips subsequently are mounted to a substrate 9 to form a package module. Alignment between Ho's LSI chips mounted on substrate 9 is within a first alignment tolerance range (e.g., within the alignment tolerance range of a chip placement tool) and alignment between the integrated structures respectively supported by different LSI chips is within a second alignment tolerance range that includes alignment mismatches between the LSI chips

mounted on substrate 9 and the alignment mismatches between the integrated structures and their supporting the LSI chips. Accordingly, the alignment tolerance range between the integrated structures respectively supported by different LSI chips in Ho's approach is larger than the alignment range between the LSI chips because of the accumulation of alignment errors.

2. Yao

The Examiner has cited Yao for his disclosure of "integrated circuit chips 30 adhered to a carrier substrate 20 using an adhesive bond 50." Yao, however, like Ho, fails to teach or suggest a common carrier in which alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures respectively supported by different integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as now recited in independent claim 1. Indeed, in Yao's approach, integrated structures are formed on substrates to form chips 30, and chips 30 subsequently are mounted to substrate 20. Accordingly, alignment between the integrated structures respectively supported by different chips 30 is within a larger alignment tolerance range than the alignment between the substrates of the chips 30 because of the accumulation of alignment errors, for the same reasons explained above in connection with Ho.

3. Ferri

Ferri discloses a microwave backdiode microcircuit that includes a single diode assembly chip 20 mounted on a dielectric substrate 14. Accordingly, Ferri does not teach or suggest anything about the alignment between a plurality of integrated chip substrates, nor anything about the alignment between integrated structures respectively supported by different integrated chip substrates.

4. Houston

Houston merely discloses a method of making a single integrated circuit chip. Accordingly, like Ferri, Houston does not teach or suggest anything about the alignment between a plurality of integrated chip substrates, nor anything about the alignment between integrated structures respectively supported by different integrated chip substrates.

5. Conclusion

For at least the reasons explained above, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri and Houston now should be withdrawn.

B. Dependent Claims 2-13 and 22-25

In the Final Office action dated December 2, 2003, the Examiner merely copied almost verbatim the text of her rejections from the prior Office action dated June 4, 2003. In response to Applicant's arguments presented in the Amendment dated September 2, 2003, the Examiner merely indicated that:

> Applicant's arguments filed 09-08-03 have been fully considered but they are not persuasive.
>
> It is within the level of ordinary skill that the tolerances between integrated circuit chip substrates are larger than the tolerance between the integrated structures on the chip substrates.

These unsubstantiated assertions, however, only addresses the limitations of independent claim 1. The Examiner has failed to address the points raised in the Amendment dated of September 2, 2003, for each of the dependent claims argued separately from claim 1. In her next action, Applicant respectfully requests that the Examiner give due consideration to each of these points, which are explained in greater detail below.

1. Claims 2 and 3

The Examiner has rejected claims 2 and 3 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri, Houston, and Akram (U.S. 2001/0014488). The Examiner has cited Akram for his disclosure of "a carrier substrate 102, an adhesive 112, and an integrated circuit chip 104." Akram, however, like Ho, fails to teach or suggest a common carrier in which alignment between integrated chip substrates is within a first alignment tolerance range and alignment between integrated structures *respectively* supported by *different* integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range, as recited in independent claim 1. Indeed, in Akram's approach, integrated structures are formed on substrates to form chips 104, and the chips 104 subsequently are mounted to substrate 102. Accordingly, alignment between the integrated structures respectively supported by different integrated circuit chips is within a larger alignment tolerance range than the alignment between the integrated circuit chips because of the

accumulation of alignment errors, for the same reasons explained above in connection with Ho.

Thus, dependent claims 2 and 3 are patentable for at least the same reasons explained above in connection with independent claim 1.

2. Claims 4-9 and 12-13

The Examiner has rejected claims 4-9 and 12-13 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri and Houston. Claims 4-9 and 12-13 incorporate the features of independent claim 1 and therefore are patentable for at least the same reasons explained above. Claims 5, 6, and 13 also are patentable for the following additional reasons.

Claim 5 recites that the carrier substrate includes a plurality of slots each containing a respective integrated chip. The Examiner has asserted that Ho's "carrier substrate includes a plurality of slots 11." Contrary to the Examiner's assertion, however, the elements 11 of Ho's package module are merely square peripheral areas 11 of substrate 9 that are used "for the fan-out of connections to pads for engineering change connections and for testing" (col. 2, lines 66-67). FIG. 2 shows a portion of the substrate of FIG. 1 with a chip removed (see col. 2, lines 25-30). *FIG. 2 of Ho clearly shows that peripheral areas 11 are merely planar surface areas of substrate 9 supporting a series of pads connected to respective solder balls in a solder ball connection area where an IC chip 10 is to be mounted.* The peripheral areas 11 are not slots that contain respective integrated chips, contrary to the Examiner's assertion. For at least this additional reason, the Examiner's rejection of claim 5 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri and Houston should be withdrawn.

Claim 6 incorporates the features of dependent claim 5 and therefore is patentable for at least the same reasons. Claim 6 additionally recites that the upper surface of the carrier substrate and upper surfaces of the integrated chips are substantially coplanar. The Examiner has asserted that "Ho further teach that the carrier substrate and the integrated chips each having parallel top surfaces which reside essentially within the same plane (Figure 1) and the carrier substrate and the integrated chips each having parallel top surfaces which do not reside within the same plane (Figure 3)." Figures 1 and 3 are top views of package modules and, therefore, do not show anything about whether or not the upper surfaces of chips 10 and the upper surface of substrate 9 are coplanar. Nevertheless, contrary to the Examiner's assertion, Ho clearly teaches that each chip 10 is mounted on substrate 9 (see, e.g., col. 2, lines 63-65; also see the solder ball connection area 30 where an IC chip is mounted to

substrate 9). Therefore, the upper surfaces of chips 10 and the upper surface of substrate 9 necessarily are not substantially coplanar. For at least this additional reason, the Examiner's rejection of claim 6 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri and Houston should be withdrawn.

Claim 13 recites that each of the plurality of integrated chips is a component of a respective inkjet print head. None of the cited references teaches of suggests such a feature. For at least this additional reason, the Examiner's rejection of claim 13 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri and Houston should be withdrawn.

4. Claim 10

The Examiner has rejected claim 10 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri, Houston, and Bayan (U.S. 6,372,359). Claim 10 incorporates the features of independent claim 1 and dependent claim 5 and, therefore, is patentable for at least the same reasons explained above. Claim 10 also is patentable for the following additional reason.

The Examiner has cited Bayan for the disclosure of "a filler material 225 adapted to fill a peripheral gap between the interior edges of each of the slots 208 and the peripheral edges of each of the integrated chips 220 when each chip is adhered within each slot." Claim 10, however, recites that each slot contains a respective integrated chip. In Bayan's approach, none of the dice 220 is contained within a trough 208. Accordingly, in Bayan's approach, there is no "filler material disposed in each peripheral gap between interior edges of each slot and peripheral edges of each respectively contained integrated chip," as recited in claim 10.

For at least this additional reason, the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri, Houston, and Bayan should be withdrawn.

5. Claim 11

The Examiner has rejected claim 11 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri, Houston, Banyan, and Moser (U.S. 4,797,780). Claim 11 incorporates the features of independent claim 1 and dependent claims 5 and 10 and, therefore, is patentable for at least the same reasons explained above. The Examiner has cited Moser for teaching "a filler material comprising glass frit." Moser, however, fails to make up for the failure of Ho, Ferri, Houston, and Bayan to teach or suggest the invention recited in claim 10, as explained above. For at least this reason, the Examiner's rejection of claim 11 under 35 U.S.C. § 103(a) over Ho in view of Yao, Ferri, Houston, Banyan, and Moser should be withdrawn.

III. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

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Respectfully submitted,

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